



TFT LCD DISPLAY MODULE

Product Specification

Customer	Standard	
Product Number	DMT024QVNXCM1-1A	
Customer Part Number		
Customer Approval		Date:

Internal Approvals		
Product Mgr	Doc. Control	Electr. Eng.
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Date: 25/10/2018	Date: 25/10/18	Date: 25/10/18

Revision Record

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	25/10/18	--	--	Initial Release	



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1.0 General Description

1.1 Introduction

This is a colour active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.4'TFT-LCD contains 240X320 pixels and can display up to 65K/262K colours.

1.2 Main Features

Item	Contents
Screen Size	2.4" Diagonal
Display Format	240 x RGB x 320 Dots
N° of Colour	65K/262K colours
Overall Dimensions	42.72 mm(H) x 60.40 mm(V) x 3.57 mm (D)
Active Area	36.72 mm (H) x 48.96 mm (V)
Display Mode	Transmissive / Normally Black
Viewing Direction	All
TFT Interface	3SPI+16/18Bit RGB
PCT Interface	I2C
TFT Driver IC	ST7789V
PCT Controller IC	FT6336U
Backlight Type	LED, White, 4 chips
Operating Temperature	-20C ~ +70°C
Storage Temperature	-30°C ~ +80°C
Module Bonding Technology	Optical Bonding
ROHS	Compliant to 2011/65/EU



2.0 Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	240 x RGB x 320 Dots	Dots
Overall Dimensions	42.72 mm(H) x 60.40 mm(V) x 3.57 mm(D)	mm
Active Area	36.72 mm (H) x 48.96 mm (V)	mm
Pixel Pitch	0.153 (H) x 0.153 (V)	mm
Weight	TBD	g

3.0 Electrical Specification

3.1 Absolute Maximum Ratings

3.1.1 TFT

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	4.6	V	-
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V	-
Operating Temperature	T _{OP}	-20	+70	°C	-
Storage Temperature	T _{ST}	-30	+80	°C	-

(Ta=25 VSS=0V)

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

3.1.2 PCT

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
Operating Temperature	T _{OP}	-20	+70	°C	-
Storage Temperature	T _{ST}	-30	+80	°C	-

Note 1: If used beyond the absolute maximum ratings, FT6336U may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

3.2 Electrical Characteristics

3.2.1 TFT

Item	Symbol	Min.	Typ.	Max.	Unit
Digital Supply Voltage	V _{CI}	2.4	3.3	3.6	V
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V
Normal Mode Current Consumption	IDD	-	5	-	mA
High Level Input	V _{IH}	0.7xI _{OVCC}	-	I _{OVCC}	V
Low Level Input	V _{IL}	GND	-	0.3xI _{OVCC}	V
High Level Output	V _{OH}	0.8I _{OVCC}	-	I _{OVCC}	V
Low Level Output	V _{OL}	GND	-	0.2xI _{OVCC}	V

3.2.2 PCT

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	2.8	3.3	3.6	V
Normal operation mode Current consumption	I _{opr}	-	4	-	mA
Monitor mode Current consumption	I _{mon}	-	1.5	-	mA
Sleep mode Current consumption	I _{slp}	-	50	-	μA
High Level Input	V _{IH}	0.75xV _{DDIO}	-	V _{DDIO}	V
Low Level Input	V _{IL}	-0.3	-	0.3xV _{DDIO}	V
High Level Output	V _{OH}	0.7xV _{DDIO}	-	-	V
Low Level Output	V _{OL}	-	-	0.3xV _{DD}	V

3.4 Interface Pin Assignment

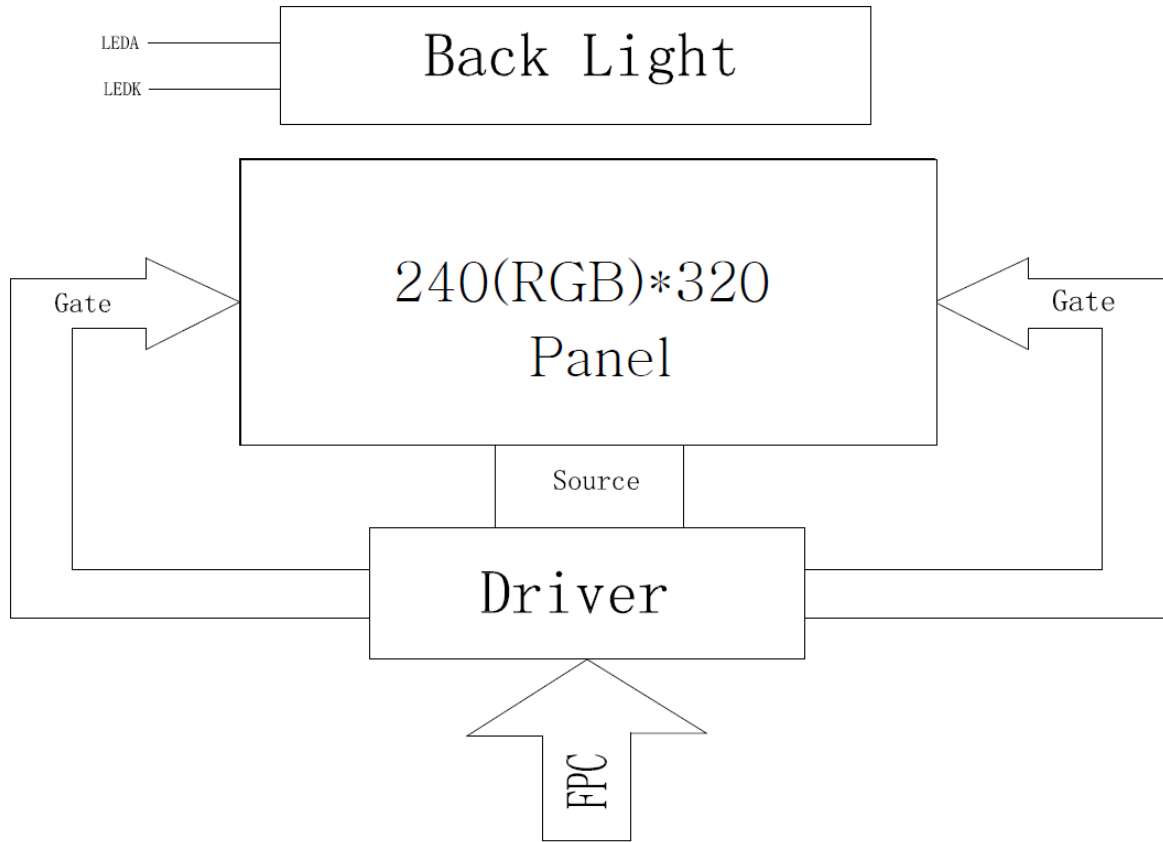
3.4.1 TFT Pin Assignment

No.	Symbol	Function
1	GND	Ground of Logic Circuit. This is a ground pin, to be connected to external ground.
2	DOTCLK	Dot clock signal for RGB interface operation. If not used please fix this pin at IOVCC or DGND.
3	GND	Ground of Logic Circuit. This is a ground pin, to be connected to external ground.
4	VSYNC	Vertical (Frame) synchronising input signal for RGB operation. If not used please fix this pin at IOVCC or DGND.
5	HSYNC	Horizontal (Line) synchronising input signal for RGB operation. If not used please fix to IOVCC or DGND.
6	ENABLE	Data enable signal for RGB interface operation. If not used please fix this pin at IOVCC or DGND.
7-16	DB17-DB8	DB17-DB8 are used as RGB interface data bus. 16-bit RGB I/F: DB17-DB13, DB11-DB1 are used. 18-bit RGB I/F: DB17-DB0 are used.
17	IOVCC	Supply voltage for IO. (1.65V-3.3V).
18-25	DB7-DB0	DB7-DB0 are used as RGB interface data bus.
26	CS	Chip select input pin ("Low" enable).
27	SCL	This pin is used serial interface clock in 4-wire 8-bit serial data interface. Fix this pin at VCI or GND when not in use.
28	SDI	SPI interface input pin. The data is latched on the rising edge of the SCL signal. If not used please fix this pin at IOVCC or DGND level.
29	RESET	Setting either pin low initializes the LSI. Must be reset after power is supplied.
30	VCI	Supply voltage (3.3V)
31	SDO	SPI interface output pin. The data is output on the falling edge of the SCL signal. If not uses leave the pin not connected.
32	LED+	Anode pin of backlight.
33	GND	Ground of Logic Circuit. This is a ground pin, to be connected to external ground.
34	LED-	Cathode pin of backlight.
35	GND	Ground of Logic Circuit. This is a ground pin, to be connected to external ground.

3.4.2 PCT Pins Assignment

No.	Symbol	Function
1	VDD	Supply voltage.
2	SCL	I2C clock input.
3	SDA	I2C data input and output.
4	INT	External interrupt to the host.
5	RST	External Reset, Low is active.
6	GND	Ground.

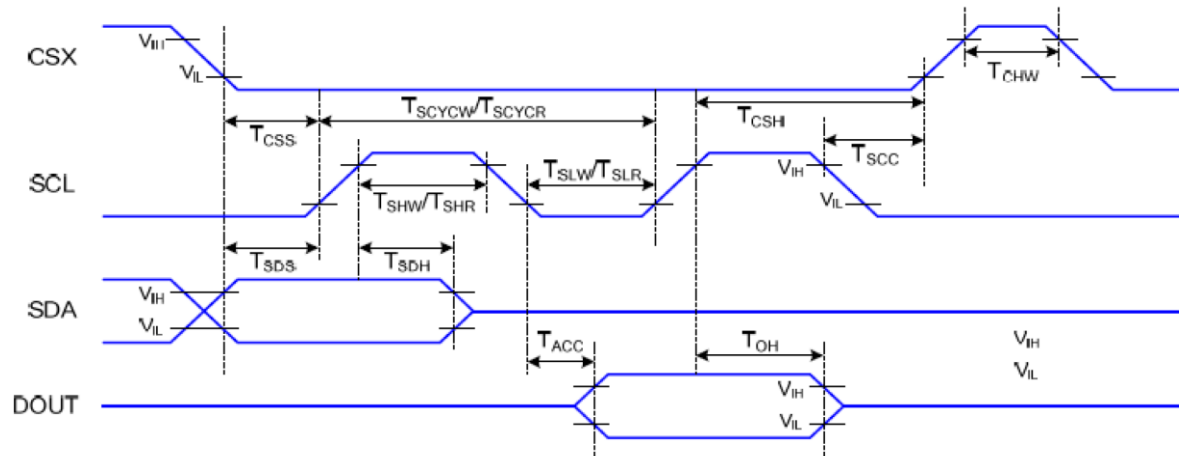
3.5 Block Diagram



3.6 Timing Characteristics

3.6.1 TFT

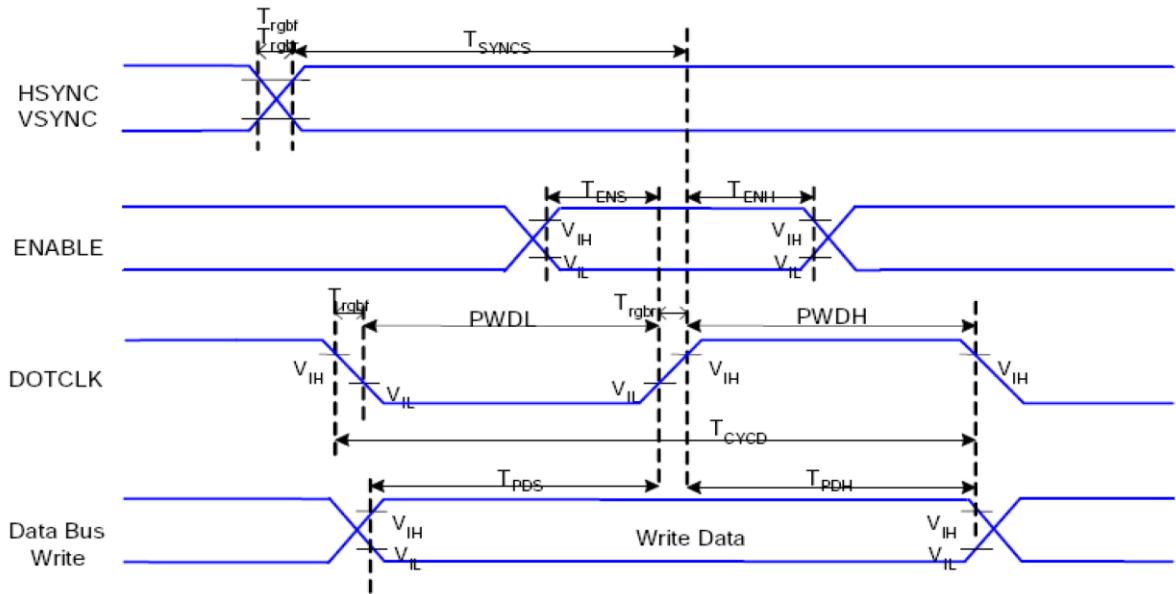
3.6.1.1 Serial Interface Characteristics (3-line serial)



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70°C

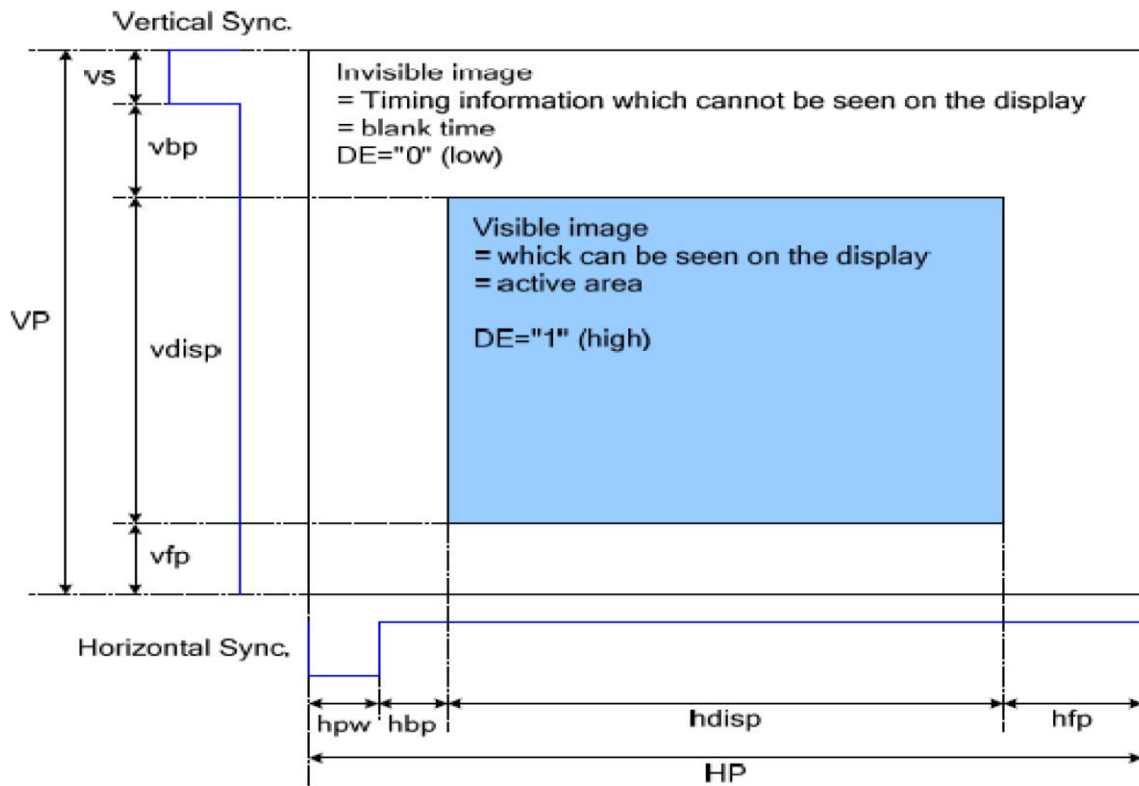
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15	-	ns	
	T_{CSH}	Chip select hold time (write)	15	-	ns	
	T_{CSS}	Chip select setup time (read)	60	-	ns	
	T_{SCC}	Chip select hold time (read)	65	-	ns	
	T_{CHW}	Chip select "H" pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66	-	ns	
	T_{SHW}	SCL "H" pulse width (write)	15	-	ns	
	T_{SLW}	SCL "L" pulse width (write)	15	-	ns	
	T_{SCYCR}	Serial clock cycle (read)	150	-	ns	
	T_{SHR}	SCL "H" pulse width (read)	60	-	ns	
	T_{SLR}	SCL "L" pulse width (read)	60	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	10	-	ns	
	T_{SDH}	Data hold time	10	-	ns	
DOUT	T_{ACC}	Access time	10	50	ns	For max.
	T_{OH}	Output disable time	15	50	ns	CL=30pF For min. CL=8pF

3.6.1.2 RGB Interface Characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	T_{rghr} , T_{rghf}	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and the front porch are used to set the RGB interface timing.



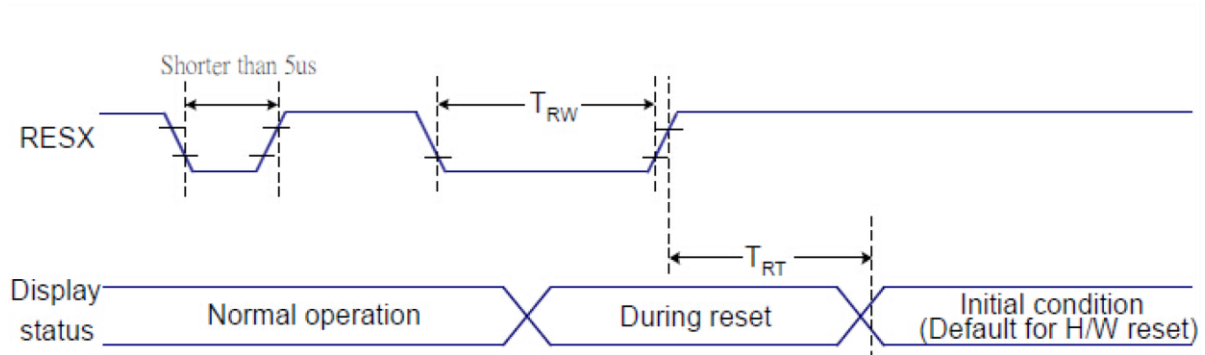
Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	10	hpw+hbp=31	Clock
Horizontal Sync. Back Porch	hbp	4	10		Clock
Horizontal Sync. Front Porch	hfp	2	38	-	Clock
Vertical Sync. Width	vs	1	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	1	4		Line
Vertical Sync. Front Porch	vfp	1	8	-	Line

Note:

1. Typical values are related to the setting of dot clock of 7MHz and frame rate is 70Hz.
2. If the setting of hpw is 10 dot clocks and hbp is 10 dot clocks, the setting of hbp in command B1h is 20 dot clocks.
3. In with ram mode, $hpw+hbp+hfp \geq 22$

3.6.1.3 Reset Timing



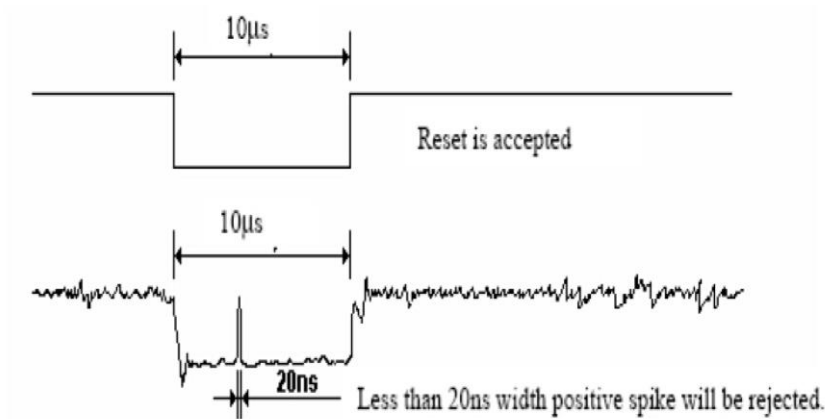
Related Pins	Symbol	Parameter	Min.	Max.	Unit
RESX	TRW	Reset pulse duration	10	-	µs
	TRT	Reset cancel	-	5(Note 1,5)	ms
			-	120(Note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9 µs	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts is Sleep Out-mode. The display remains the blank state in Sleep In-mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset is applied during Sleep In Mode.
6. When Reset applied during Sleep Out Model.
7. It's necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.

3.6.2 PCT

3.6.2.1 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V; Ta=25°C	34.65	35	35.35	MHz	

AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V; Ta=25°C	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V; Ta=25°C	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V; Ta=25°C	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V; Ta=25°C	-	5	-	V	

3.6.2.2 I2C Interface

The I2C is always configured in the Slave mode. The data transfer format is shown in figure 4-1.

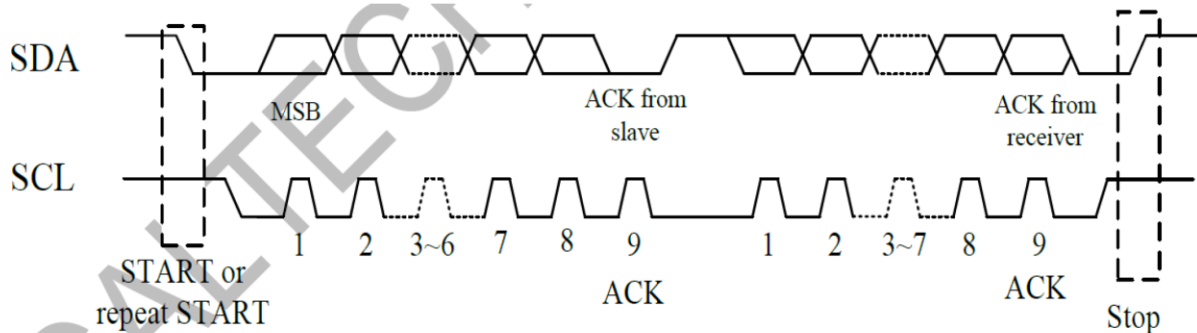


Figure 4-1 I2C Serial Data Transfer Format

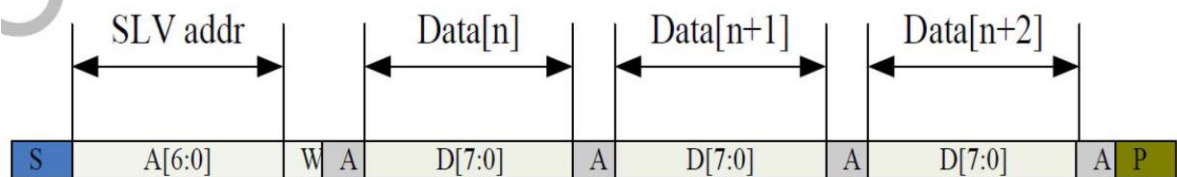


Figure 4-2 I2C master write, slave read

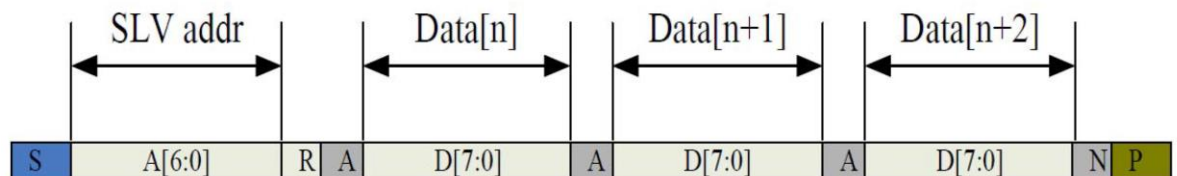


Figure 4-3 I2C master read, slave write

Table 4-3 lists the meanings of the mnemonics used in above figures.

Table 4-3 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics are shown in table 4-4.

Table 4-4 I2C Timing Characteristics

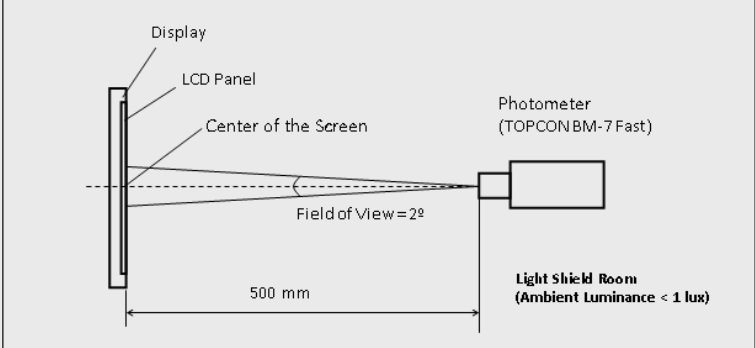
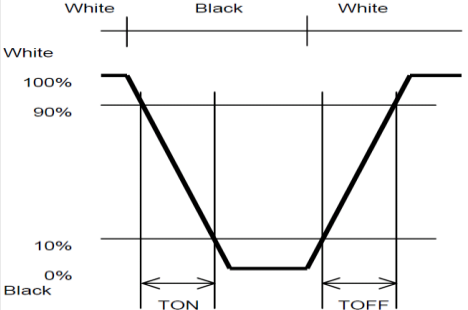
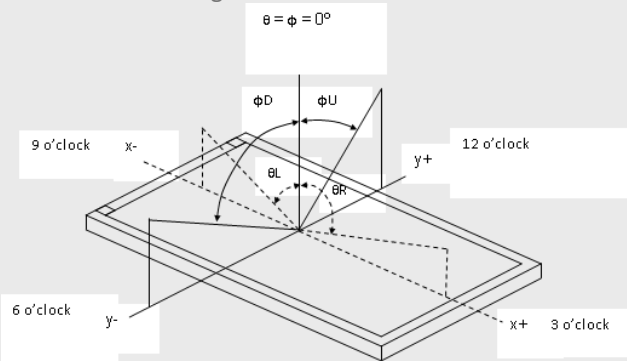
Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

4.0 Optical Specification

4.1 Optical Characteristics

Measuring instruments: LCD-5100, Eldim, Topcon BM-7
 Driving condition: $V_{DD} = 3.3V$, $V_{SS} = 0V$
 Backlight: $IF = 75mA$
 Measured temperature: $T_a = 25^{\circ}C$

Characteristics		Symbol	Conditions	Min	Typ	Max	Unit	Note
Response time		TR+TF	$\theta = \phi = 0^{\circ}$ Normal	-	35	45	ms	2
Contrast Ratio		CR	Viewing Angle	640	800	-	-	3
Uniformity		S(%)		-	70	-	%	
Viewing Angle	Left	θ_L	CR \geq 10	-	80	-	deg	4
	Right	θ_R		-	80	-		
	Up	θ_U		-	80	-		
	Down	θ_D		-	80	-		
Colour Chromaticity	Red	Rx	CR \geq 10	0.5931	0.6331	0.6731	-	5
		Ry		0.2936	0.3336	0.3736		
	Green	Gx		0.2822	0.3222	0.3622		
		Gy		0.5718	0.6118	0.6518		
	Blue	Bx		0.1084	0.1484	0.1884		
		By		0.0034	0.0434	0.0834		
	White	Wx		0.3585	0.2985	0.3385		
		Wy		0.2786	0.3186	0.3586		
Option View Direction			All					

Note	Item	Test method
1	Setup	<p>The display should be stabilised at a given temperature for 30 minutes to avoid abrupt temperature change during measuring. To stabilise the luminance, measurements should be executed after lighting the backlight for 30 minutes in a windless room.</p> 
2	Response time	<p>Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white.</p> 
3	Contrast ratio	<p>Measure maximum brightness and minimum brightness at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values.</p> $\text{Contrast Ratio (CR)} = \frac{\text{Brightness of unselected position (white)}}{\text{Brightness of selected position (black)}}$
4	Viewing angle Horizontal θ Vertical ϕ	<p>Move the luminance meter from right to left and up and down and determine the angles where contrast ratio is 10</p> 
5	Colour chromaticity	<p>Measure chromaticity coordinates x and y of CIE1931 colorimetric system</p>
6	Brightness distribution	<p>(Brightness distribution) = $100 \times B/A \%$ A: max. brightness of the 9 points B: min. brightness of the 9 points</p>

5.0 LED Backlight Specification

5.1 LED Backlight Characteristics

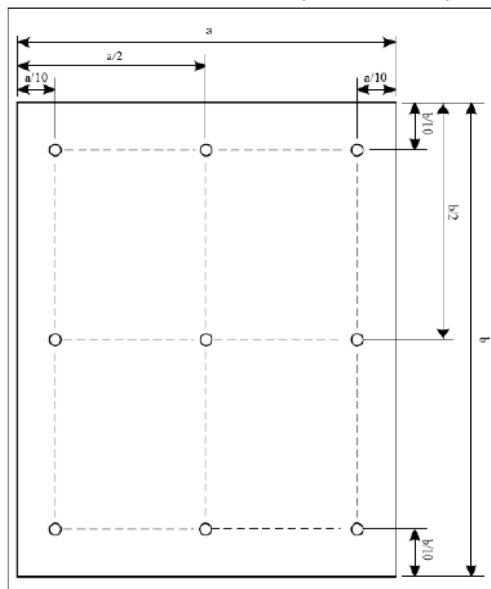
The back-light system is edge-lighting type with 4 chips LED

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	I_F	15	20	-	mA	-
Forward Voltage	V_F	-	12.8	-	V	-
LCM Luminance	LV	330	380	-	Cd/m ²	3
LED life time	Hr	50000	-	-	Hour	1,2
Uniformity	Avg	80	-	-	%	3

Note 1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: $T_a=25\pm 3$ °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at $T_a=25$ °C and $I_L=80$ mA. The LED lifetime could be decreased if operating I_L is larger than 80mA. The constant current driving method is suggested.

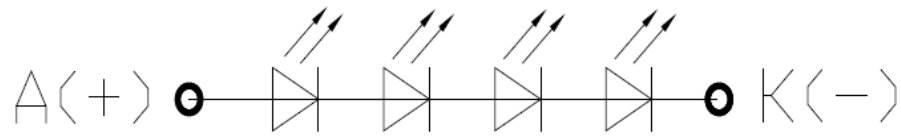
Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

5.2 Internal Circuit Diagram



BLU CIRCUIT DIAGRAM

6.0 Quality Assurance Specification

6.1 Delivery Inspection Standards

6.1.1 Inspection Conditions

Inspection distance: 30 cm - 50cm
Viewing angle: $\pm 45^\circ$

6.1.2 Environmental Conditions

Ambient temperature: $25^\circ\text{C} \pm 5^\circ\text{C}$
Ambient humidity: $65 \pm 10\% \text{ RH}$
Ambient illumination: 300~700 lux

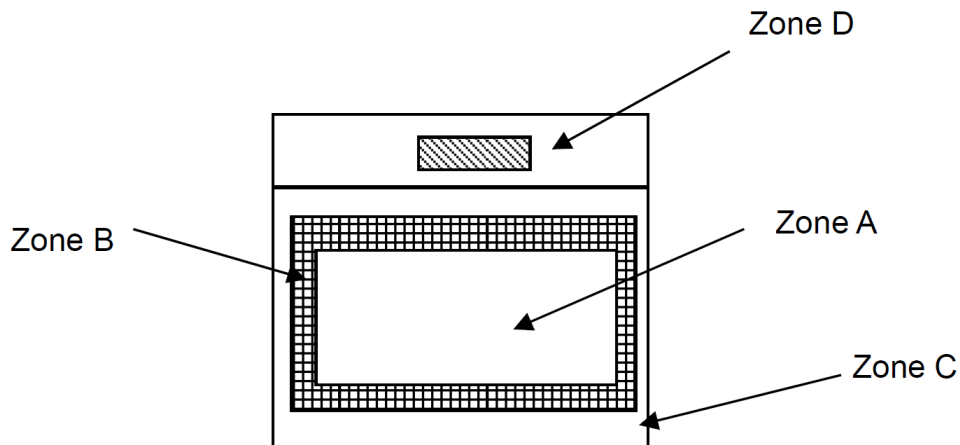
6.1.3 Sampling Conditions

1. Lot size: quantity of shipment lot per model
2. Sampling method:

Sampling plan		GB/T 2828-2003
		Normal inspection, Class II
AQL	Major Defect	0.65%
	Minor Defect	1.5%

No.	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Colour tone	Colour unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot, Dim spot, Polarizer bubble; Polarizer accidented spot.	
6	Soldering appearance	Good soldering, peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

6.1.4 Zone Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (ZoneA+ZoneB) which can't be seen after assembly by customer.

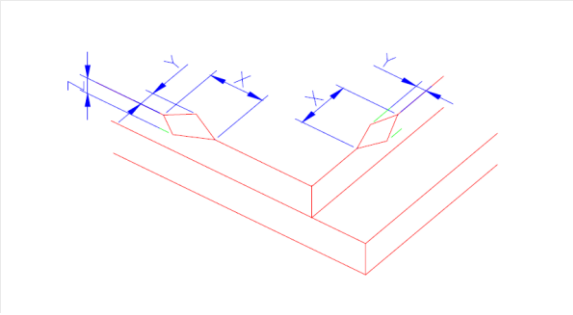
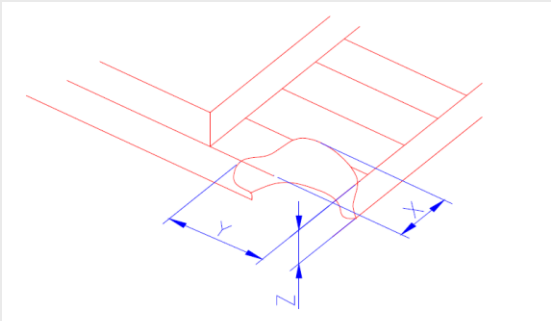
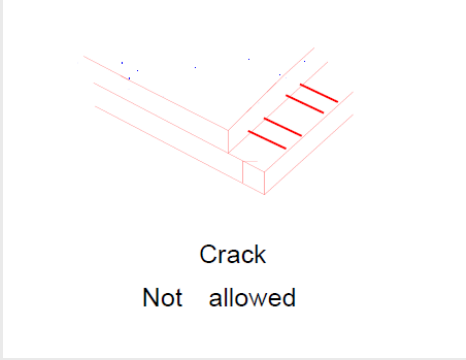
Zone D: IC Bonding Area

Note: Generally, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer.


6.1.5 Basic Principle


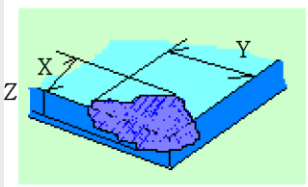
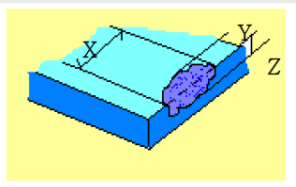
A set of sample to indicate the limit of acceptable quality level shall be discussed should a dispute occur.

6.1.6 Inspection Criteria

Number	Items	Criteria (mm)			
1.0 LCD Crack/ Broken	(1) The edge of LCD broken				
		X	Y	Z	
	Note: X: Length Y: Width Z: Height L: Length of ITO T: Height of LCD	(2) LCD corner broken			
			≤3.0mm	<Inner border line of the seal	≤T
	(3) LCD crack				

Number	Items	Criteria (mm)				
2.0	Spot defects  $\Phi = (X+Y) / 2$	① Light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)				
		Size (mm)	Zone	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.10$		Ignore		
		$0.10 < \Phi \leq 0.25$		4(distance ≥ 10 mm)		
		$0.25 < \Phi \leq 0.35$		3		
		$\Phi > 0.4$		0		
		② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)				
		Size (mm)	Zone	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.1$		Ignore		
		$0.10 < \Phi \leq 0.25$		4(distance ≥ 10 mm)		
		$0.25 < \Phi \leq 0.35$		3		
		$\Phi > 0.40$		0		
		③ Polarizer accidented spot				
		Size (mm)	Zone	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.2$		Ignore		
		$0.3 < \Phi \leq 0.5$		3(distance ≥ 10 mm)		
		$\Phi > 0.5$		1		
		④ Pixel bad points (light dot, Dim dot, colour dot)				
		Size (mm)	Zone	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.15$		Ignore		
		$0.2 < \Phi \leq 0.3$		2(distance ≥ 10 mm)		
		$\Phi > 0.4$		1		
		⑤ Polarizer Bubble				
		Size (mm)	Zone	Acceptable Qty		
		A	B	C		
$\Phi \leq 0.2$		Ignore				
$0.3 < \Phi \leq 0.4$		4(distance ≥ 10 mm)				
$0.4 < \Phi \leq 0.5$		3				
$\Phi > 0.5$		1				

3.0	Line defect (LCD/TP/ Polarizer black/ white line, scratch, stain)	Width (mm)	Length (mm)	Acceptable Qty		
		$\Phi \leq 0.05$	Ignore	A	B	C
		$0.05 < W \leq 0.06$	$L \leq 5.0$	Ignore		Ignore
		$0.07 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$		
$0.08 < W$	Define as spot defect					
4.0	SMT	Do not allow: missing parts, solderless connection, cold solder joint, miss match, the positive and negative polarity oppose				
5.0	Display colour & Brightness	1. Colour: Measuring the colour coordinates, The measurement standard according to the datasheet or samples 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples				
6.0	LCD Mura	By 5% ND filter invisible				
7.0	RTP Related	TP bubble / accidented spot				
		Size Φ (mm)	Zone	Acceptable Qty		
		$\Phi \leq 0.1$		A	B	C
		$0.1 < \Phi \leq 0.25$		Ignore		Ignore
		$0.25 < \Phi \leq 0.35$		4(distance ≥ 10 mm)		
		$0.4 < \Phi$		3		
				1		
		TP film scratch				
		Width(mm)	Length (mm)	Acceptable Qty		
		$\Phi \leq 0.05$	Ignore	A	B	C
		$0.05 < W \leq 0.06$	$L \leq 5.0$	Ignore		Ignore
		$0.07 < W \leq 0.08$	$L \leq 4.0$	$N \leq 3$		
		$0.08 < W$	Define as spot defect			
Assembly deflection	Beyond the edge of backlight ≤ 0.2 mm					
Bulge (undulation included)	The ITO film plumped below 0.40mm is acceptable					
						

Number	Items	Criteria (mm)				
5.0	RTP Related	Newton Ring	Newton Ring area > 1/3 TP area not acceptable			
			Newton Ring area ≤ 1/3 TP area acceptable			
			TP corner broken X: length Y: Width Z: Height	X	Y	
			X ≤ 3.0 mm	Y ≤ 3.0 mm	Z < LCD thickness	
Circuitry broken is not allowed						
		TP edge broken X: length Y: Width Z: Height	X	Y	Z	
			X ≤ 6.0 mm	Y ≤ 2.0 mm	Z < LCD thickness	
Circuitry broken is not allowed						

- Criteria (functional items)

Number	Items	Criteria
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed



6.2 Dealing with Customer Complaints

6.2.1 Non-conforming Analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in two weeks from receiving the sample. If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.2.2 Handling of Non-conforming Displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7.0 Reliability Specification

7.1 Reliability Tests

Test Item	Test Condition		Sample Size
High Temperature Operation	Ta= 70°C	96 h	3pcs
Low Temperature Operation	Ta = -20°C	96 h	3pcs
High Temperature Storage	Tp = 80°C	96 h	3pcs
Low Temperature Storage	Tp = -30°C	96 h	3pcs
High Temperature & High Humidity Operation	60°C, 90% RH	96 h	3pcs
Thermal Shock (Non-operation)	-30°C,30 min ↔ 80°C,30 min, Change time:5min 20CYC.		3pcs
ESD test	C=150pF, R=330,5points/panel Air: ±8KV, 5times; Contact: ±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).		3pcs
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).		3pcs
Box Drop Test	1 Corner 3 Edge 6 faces, 80 cm (Medium Box)		1 box

Note: Ta = ambient temperature, Tp= panel temperature

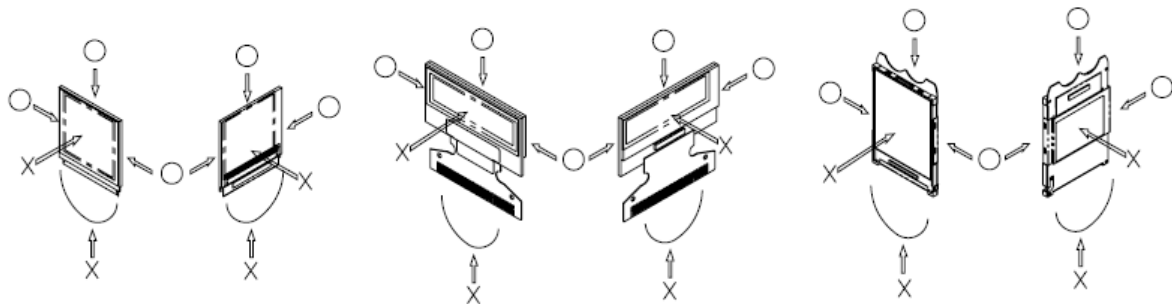
Notes:

1. No dew condensation to be observed.
2. The function test shall be conducted after 4 hours storage at the normal temperature and humidity after removed from the test chamber.
3. No cosmetic or functional defects should be allowed.
4. Total current consumption should be less than twice the initial value.

8.0 Handling Precautions

8.1 Handling Precautions

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water
- 4) If pressure is applied to the display surface or its neighbourhood of the display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 5) The polarizer covering the surface of the display module is soft and easily scratched. Please be careful when handling the display module.
- 6) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
 - a. Scotch Mending Tape No. 810 or an equivalent
2. Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
3. Also, pay attention that the following liquid and solvent may spoil the polarizer:
 - Water
 - Ketone
 - Aromatic Solvents
- 7) Hold the display module very carefully when placing it into the system housing. Do not apply excessive stress or pressure to display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- 8) Do not apply stress to the LSI chips and the surrounding molded sections.
- 9) Do not disassemble nor modify the display module.
- 10) Do not apply input signals while the logic power is off.
- 11) Pay sufficient attention to the working environments when handling display modules to prevent occurrence of element breakage accidents by static electricity.
 - Be sure to make human body grounding when handling display modules.
 - Be sure to ground tools to use or assembly such as soldering irons.
 - To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

- Protective film is being applied to the surface of the display panel of the display module. Be careful since static electricity may be generated when exfoliating the protective film.
- 12) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. If the display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
 - 13) If electric current is applied when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

- 1) When storing display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
- 2) If electric current is applied when water drops are adhering to the surface of the display module, when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

- 1) The absolute maximum ratings are the ratings which cannot be exceeded for display module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the display module, fasten the external plastic housing section.
- 7) If power supply to the display module is forcibly shut down by such errors as taking out the main battery while the display panel is in operation, we cannot guarantee the quality of this display module.

8.4 Operation Precautions

- 1) It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.
- 2) Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Consider prevent direct current during ON/OFF timing and during operation.
- 3) Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged.
- 4) To protect display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the display modules.
 - Pins and electrodes
 - Pattern layouts such as the FPC
- 5) When the driver is being exposed (COG), semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if the driver is exposed to light, malfunctioning may occur.
 - Design the product and installation method so that the driver may be shielded from light in actual usage.
 - Design the product and installation method so that the driver may be shielded from light during the inspection processes.
- 6) Although the display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- 7) We recommend you construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

8.5 Other Precautions

Request the qualified companies to handle industrial wastes when disposing of the display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.